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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,783	03/12/2004	Jin-Kyoung Jung	SAM-0529	8323

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Steven M. Mills
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,783	JUNG ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7-12,14-23 and 25-38* is/are pending in the application.

4a) Of the above claim(s) *4-6,13,17-22,24 and 26* is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,7-9 and 30-38* is/are allowed.

6)☒ Claim(s) *10-12, 14-16, 23,25 and 27- 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/12/2004 and 8/18/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 4/18/2006 has been received and entered in the case.

2. The indicated allowability of claim 10 is withdrawn in view of the newly discovered reference(s) to Yamatasaki in view of Sher. Rejections based on the newly cited reference(s) follow.

Claim Objections

3. Claim 28 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 28 is dependent on claim 1 and 23. For purposes of the examination claim 28 is assumed to depend from claim 23 only.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10-12, 14-17, 23, 25 and 27-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki (20020053943) in view of Sher (US 6633196).

With respect to claim 10, figure 1 and 5a of Yamasaki discloses a semiconductor device comprising; a control signal generating circuit (5a) for generating a control signal (TE) responsive to an input signal (/RAS, /CAS, /WE or Add) related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits; and an internal voltage generating circuit (Figure 1) coupled to the control signal generating circuit for receiving the control signal (TE), the internal voltage generating circuit comprising a comparing circuit (CMP) for comparing a reference voltage (Vref) to an internal voltage (IntVcc) to generate a comparing signal; a switching circuit (DR) for transmitting the comparing signal as a driving signal when the control signal (TE) is inactivated and a driving signal control circuit (2) for inactivating the driving signal when the control signal is activated and an internal voltage driving circuit (RFG, Figure 20) for receiving an external power voltage (EX) and generating the internal voltage in response to the driving signal but fails to disclose wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated. Figures 3a and 3b of Sher teaches the use of CMOS transmission gates for NMOS transistor switching elements. It would have been obvious at the time the invention was made to one of ordinary skill in the art to

substitute the NMOS switching elements of Yamasaki with CMOS transmission gates for the purpose of improving switching speed.

With respect to claim 11, the above circuit produces the circuit of claim 10 wherein the driving signal control circuit includes an NMOS transistor (2f) which has a drain connected to the driving signal generating terminal (via 2ba) for generating the driving signal, a gate to which the control signal (TE) is applied, and a source connected to a ground voltage.

With respect to claim 12, the above circuit produces the circuit of claim 10 wherein the internal voltage driving circuit includes a PMOS transistor (DR) which has a source to which the external power voltage is applied (EX) a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage (IntVcc) wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to an external power voltage when the driving signal is inactivated.

With respect to claim 14, the above circuit produces the circuit of claim 10 but fails to produce the circuit wherein the input signal is generated using a fuse. It is well known in the art to use a laser burned fuse to generate an irreversible signal that can be controlled externally. It would have been obvious at the time the invention was made to one of ordinary skill in the art to use a fuse to generate an input signal for the purpose of making the input signal irreversible.

With respect to claim 15, the recitation of the input signal being generated by an external pad is deemed to be inherent because in a semiconductor device an external pad is inherently used to connect to circuits.

With respect to claim 16, the circuit above produces the circuit of claim 23, wherein the control signal generating circuit (5a) activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command. (See paragraphs [0093] and [0094]).

With respect to claim 23, figure 1 and 5a of Yamasaki discloses a control signal generating circuit (5a) for generating a control signal (TE) responsive to an input signal (/RAS, /CAS, /WE or Add) related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits; and an internal voltage generating circuit (Figure 1) coupled to the control signal generating circuit for receiving the control signal (TE) and comparing a reference voltage (Vref) to an internal voltage (IntVcc) to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, and to make the internal voltage have an external power voltage level when the control signal is activated, wherein the internal voltage generating circuit comprises at least one of a first switching circuit (2e) that cuts off an external power voltage applied to the internal voltage generating circuit when the

control signal (TE) is activated, a second switching circuit (2f) that cuts off a ground voltage supplied to the internal voltage generating circuit when the control signal (TE) is activated and a third switching circuit (2c) but fails to disclose the third switching circuit including a CMOS transmission gate which transmits the driving signal when the control signal is inactivated. Figures 3a and 3b of Sher teaches the use of CMOS transmission gates for NMOS transistor switching elements. It would have been obvious at the time the invention was made to one of ordinary skill in the art to substitute the NMOS switching elements of Yamasaki with CMOS transmission gates for the purpose of improving switching speed.

With respect to 25, the circuit above produces the circuit of claim 23, wherein the internal voltage generating circuit includes a comparing circuit (CMP) for comparing the reference voltage to the internal voltage (IntVcc) to generate a comparing signal; a switching circuit (DR) for transmitting the comparing signal as a driving signal when the control signal is control signal is inactivated; a driving signal control circuit (2) for inactivating the driving signal when the control signal is activated and an internal voltage driving circuit (RFG, Figure 20) for receiving an external power voltage (EX) and generating the internal voltage in response to the driving signal.

With respect to claim 27, the above circuit produces the circuit of claim 23 but fails to produce the circuit wherein the input signal is generated using a fuse. It is well known in the art to use a laser burned fuse to generate an irreversible signal that can be controlled externally. It would have been obvious at the time the invention was made to

one of ordinary skill in the art to use a fuse to generate an input signal for the purpose of making the input signal irreversible.

With respect to claim 28, the recitation of the input signal being generated by an external pad is deemed to be inherent because in a semiconductor device an external pad is inherently used to connect to circuits.

With respect to claim 29, the circuit above produces the circuit of claim 23, wherein the control signal generating circuit (5a) activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command. (See paragraphs [0093] and [0094]).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KEA
7/25/2006

Quan Tra
Primary Examiner